Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1 (currently amended): A connection device capable of converting a pixel clock to a character clock, the connection device comprising:

a pixel clock generator for generating a pixel clock having a number of cycles that is not an integer multiple of a first number during a predetermined interval;

a frequency divider for generating a character clock according to the pixel clock; and

a logic unit directly connected to the frequency divider for controlling the frequency divider to generate the character clock by dividing the number of cycles of the pixel clock during part of the predetermined interval by the first number, division of the number of cycles of the pixel clock during the predetermined interval by the first number producing a quotient and a remainder, the remainder being equal to a second number of remaining pixel clocks, the logic unit adding one or more extra cycles of the pixel clock to cycles of the character clock during the predetermined interval until the second number of remaining pixel clocks have all been added to cycles of the character clock, wherein the second number is less than the first number and both the first and second numbers are positive integers ~~and by dividing the number of cycles of the pixel clock during the remaining part of the predetermined interval by a second number~~.

2 (currently amended): The connection device of claim 1 wherein durations of both high and low states of the character clock are multiples of the pixel clock period ~~the logic unit makes the number of cycles of the character clock generated by the frequency divider an integer~~.

3 (original): The connection device of claim 1 wherein the first number is eight or nine.

4 (cancelled).

5 (currently amended): A method for converting a pixel clock to a character clock, the method comprising:

providing a pixel clock with a number of cycles that is not an integer multiple of a first number during a predetermined interval; [[and]]

dividing the number of cycles of the pixel clock during part of the predetermined interval by the first number, division of the number of cycles of the pixel clock during the predetermined interval by the first number producing a quotient and a remainder, the remainder being equal to a second number of remaining pixel clocks, wherein the second number is less than the first number and both the first and second numbers are positive integers; and

~~and dividing the number of cycles of the pixel clock during the remaining part of the predetermined interval by a second number for generating the character clock~~

the logic unit adding one or more extra cycles of the pixel clock to cycles of the character clock during the predetermined interval until the second number of remaining pixel clocks have all been added to cycles of the character clock.

6 (currently amended): The method of claim 5 wherein durations of both high and low states of the character clock are multiples of the pixel clock period ~~the number of cycles of the character clock generated by dividing the pixel clock during the predetermined interval is an integer~~.

7 (original): The method of claim 5 wherein the first number is eight or nine.

8 (cancelled).